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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,379	09/17/2003	Darrin Benzer	13546US02	4562

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,379	BENZER ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/17/03 + 11/1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The pre-amendment filed on 9/17/03 is non-compliant because the abstract is not presented on a separate sheet, see 37 CFR 1.72.

Specification

2. The abstract of the disclosure is objected to because the abstract in the pre-amendment filed on 9/17/03 is not on a separate sheet. Note that the amended abstract was presented on the same page with the amendment to the specification. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claims 20-24 are objected to because of the following informalities:

Claim 20, line 2, "another using [a single-ended input]" should be changed to --another level using--.

Claim 20, line 3, "input, including" should be changed to --input, said level shifter circuit including-- to avoid a confusion in the claim.

Claim 20, line 7, "[a]" should be deleted because [a] does not means "a" to be deleted since a single bracket is used. To delete a word that less than 5 characters, it is either line through the word or use a double bracket.

Claims 21-24 are objected to because they include the minor informalities of claim 20.

Claim 23, line 2, "VOD" should be changed to --VDD--.

Appropriate correction is required.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 9-24 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,650,167. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-8 of the Patent 6,650,167 recites a level shifter having a single-ended input comprising a first native NMOS transistor device having a threshold voltage less than 0V, a second transistor device and a level shifter transistor device which meets all the method steps of claims 9-24 because with elements recited in the apparatus claims 1-8 of the U.S. Patent 6,650,167, it is obvious to one skill in the art that the elements of the apparatus also performs all the method steps recited in claims 9-24 of the instant application.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 20-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 20, the recitation "determined if the input signal is greater than a threshold value of said native NMOS transistor device" is misdescriptive because it is inconsistent with the disclosure. It is seen that the disclosure disclose the determining if the input signal is greater than the threshold voltage of the second transistor device (NMOS 310, Figure 3), not the threshold voltage of the native NMOS transistor (316, Figure 3) as recited in the claim (see paragraphs [28]-[31] and [34]-[36] of the instant specification). Further, the input signal varies from ground to Vdd, while the threshold of the native NMOS transistor is less than 0V, so it is inherent that the input signal always greater than the threshold NMOS transistor. Thus, it is suggested that "native NMOS" on line 8 of the claim be changed to --second-- to over come the 112, 2nd paragraph rejection.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 9-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano (USP 5,650,742) in view of Cress et al. (USP 6,483,386).

With respect to claims 9-15, Figure 1 of the Hirano reference discloses a level shifter circuit (101), which meets a method of translating a voltage level of a single-ended input signal

(I1) using at least one pass NMOS transistor device (Qn101) including: outputting a first voltage level if the single-ended input signal is in a first state (i.e., if the first state of the input signal I1 is at logic Lo, the output O1 of the circuit is at logic Hi; and if the first state of the input signal I1 is at logic Hi, the output O1 of the circuit is at logic Lo); and outputting a second voltage level if the single ended input is in a second state (i.e., if the first state of the input signal I1 is at logic Hi, the output O1 of the circuit is at logic Lo; and if the first state of the input signal I1 is at logic Lo, the output O1 of the circuit is at logic Hi). The Hirano reference does not disclose that the at least one pass NMOS transistor device (Qn101) is a native NMOS transistor device having a threshold voltage less than 0V. However, the Cress et al. reference discloses (note M3 in Figure 5, lines 45-65 of Col. 2, lines 18-43 of Col. 3, and lines 4-31 of Col. 4 of Cress et al.) a pass transistor device (M3) is a native NMOS transistor device having a threshold voltage less than 0V (-200mV, see lines 34-36 of Col. 3 of Cress et al.) for the purpose of having an input signal fully passes through the pass NMOS transistor device because the use of a native NMOS as a pass transistor provides a signal with low signal distortion (see line 24-31 of Col. 4, Cress et al.). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 1 of the Hirano reference by specifically using the native NMOS pass transistor (M3) having a threshold voltage of less than 0V, as taught by the Cress et al. reference, for the NMOS pass transistor (Qn101, Figure 1 of Hirano) for the purpose of fully pass the input signal through the pass transistor device since native NMOS pass transistor provides a signal with low distortion. Thus, this modification meets all the limitations of these claims including the limitation that the at least one native NMOS transistor device having a threshold voltage less than 0V (-200mV as discussed above).

With respect to claim 16, the above modification of the level shifter circuit as discussed above (with regard to claim 9) meets all the limitation of this claim, i.e., the modification circuit discloses a level shifter circuit (101), which meets a method of translating a voltage level of a single-ended input signal (I1) using at least one native NMOS transistor device having a threshold voltage less than 0V (-200mv, see rejection of claim 9) including: determining if the input signal (I1) is high (input signal I1 having logic Hi, transistor Qn102 turns ON); outputting a low signal if the input signal is high (output signal O1 is a low signal if the input signal I1 is high); and outputting a high signal if the input signal is not high (Qn102 is off, and Qp102 is ON).

With respect to claim 17, the above modification meets the limitation that determining if the input signal is high includes determining if the input signal (I1) is greater than a first voltage (the threshold voltage of the n-channel transistor Qn102, i.e., the input signal I1 is considered to be Hi when the input signal I1 is greater than the threshold voltage of the enhancement n-channel transistor Qn102).

With respect to claim 18, the above modification meets the limitation that determining if the input signal (I1) is not high includes determining if the input signal is less than a second voltage (the threshold voltage of the p-channel transistor Qp102, i.e., the input signal I1 is considered to be Lo when the input signal I1 is less than the threshold voltage of the enhancement p-channel transistor Qp102, so transistor Qp102 is ON).

With respect to claim 19, the above modification meets the limitation that eliminating static current drain (the feedback transistor Qp101 in Figure 1 of the Hirano reference in the above modification, see lines 58-65 of Col. 7 of the Hirano reference).

Insofar as understood in claims 20-24, the above modification (as discussed above with regard to claim 9) meets all the limitations of these claims, i.e., the level shifter circuit having a single-end input (I1), a first native NMOS transistor (the replacement of the Qn101 transistor as discussed in claim 9) having threshold voltage of less than 0V (-200mV, see discussion in claim 9), a second transistor (Qn102), and a level shifter transistor (Qp102). Note that the method steps recited in this claim are also met including: determining if the input signal is greater than a threshold value of the second transistor (Qn102 turns ON if input signal I1 greater than threshold value of Qn102); outputting a low signal if the input signal is greater than the threshold value (Qn102 turns ON if input signal I1 greater than threshold value of Qn102, so output O1 is Lo and having a ground voltage level); outputting a Hi signal if the input signal is not greater than the threshold value (if input signal I1 is not greater than threshold value of Qn102, then Qp102 turns ON so output O1 is Hi and having a VDD level); and eliminating static current drain (by feed back transistor Qp101); and wherein outputting a high signal comprising determining if the input signal is "greater" than a second threshold value (the threshold of Qp102, because if the input I1 greater than the threshold of Qp102 then Qp102 turns off; note that Qp102 turns On when I1 is less than the threshold of Qp102); and determining if the input signal is less than the threshold value but greater than the second threshold value (the output signal is not determined Hi or Lo).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 3, 2005

Long Nguyen
Primary Examiner
Art Unit: 2816